#11

Our Docket No.: 00-479 / 1496.00052

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	Adviat M. Mogre, et al.		
Application No.:	09/726,819	Examiner:	Natnael, P.
Filed:	November 30, 2000	Art Group:	2614
For:	SYSTEM TO EFFICIENTLY TRANSMIT TWO HDTV CHANNELS OVER SATELLITE USING TURBO CODED 8PSK MODULATION FOR DSS COMPLIANT RECEIVERS		

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop - Appeal Brief Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 30, 2004.

By: Jan M. Dunbar
Jan M. Dunbar

APPEAL BRIEF

Mail Stop - Appeal Brief Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Please charge $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c) and any additional fees or credit any overpayment to Deposit Account Number 12-2252.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, LSI Logic Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6-9, 11-14, 16-19 and 21-24 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-4, 6-9, 11-14, 16-19 and 21-24.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on October 22, 2003. On December 17, 2003, Appellants filed an Amendment After Final. On January 20, 2004, the Examiner issues an Advisory Action indicating that the Amendment After Final changes would not be entered. On February 12, 2004, Appellants filed a Notice of Appeal based on the last set of claims prior to the Amendment After Final.

V. SUMMARY OF INVENTION

The present invention concerns a system generally comprising a formatter (102), an error correction encoder (104), an interleave module (106), an inserter (108) and a turbo encoder (110). The formatter may be configured to format a plurality of data frames (300) received in a transport stream (Packets from DSS Source Encoder) by inserting a plurality of synchronization data (402) to produce a block stream (404). The error correction encoder may be configured to encode the block stream to produce an error protected block stream (600). The interleave module may be configured to interleave the error protected block stream to produce a data stream (output of block 106). The inserter may be configured to insert a synchronization signal (702) into the data stream. The turbo encoder may be configured to encode the data stream to produce an encoded stream (S1, P1' and P2').

VI. ISSUES

The first issue is whether claims 22 and 24 are patentable under the 35 U.S.C. §112, first paragraph, written description criteria.

The second issue is whether claims 1-4, 6-9, 11-14, 16-19 and 21-24 under 35 U.S.C. §103(a) are patentable over Citta et al., U.S. Patent No. 5,583,889 (hereafter Citta) in view of Yi, U.S. Patent No. 6,094,427.

VII. GROUPING OF CLAIMS

Appellants contend that the claims of the present invention do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1, 3, 4, 6, 8 and 9 stand together.

Group 2: Claims 11 and 16 stand together.

Group 3: Claims 2 and 7 stand together.

Group 4: Claim 21 stands alone.

Group 5: Claim 22 stands alone.

Group 6: Claims 12 and 17 stand together.

Group 7: Claims 13 and 18 stand together.

Group 8: Claims 14 and 19 stand together.

Group 9: Claim 23 stands alone.

Group 10: Claim 24 stands alone.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups.

VIII. ARGUMENTS

A. 35 U.S.C. §112

1. Group 5 (claim 22) is patentable under 35 U.S.C.§ 112, first paragraph.

The Examiner rejected the claimed phrase "a bit error rate not greater than 2 errors per 10,000 bits" asserting no such description in the original specification.[1] In contrast, the original specification states:

> Consequently, the turbo encoder 110 following an RS(204, 188) encoding only requires a BER of approximately $2x10^{-4}$ (line 1308) to achieve the desired SNR.[2]

---

[1] Office Action, October 22, 2003, page 2, section 2, lines 6-8.

[2] Application, page 17, line 20 thru page 18, line 2.

One of ordinary skill in the art would understand that a "bit error rate of $2x10^{-4}$" may be written as "2 errors per 10,000 bits". Therefore, one skilled in the relevant art would appear to understand that the inventors had possession of the claimed invention at the time that the invention was filed. As such, the claim of group 5 is fully compliant with the 35 U.S.C. §112, first paragraph, written description criteria and the rejection should be reversed.

2. Group 10 (claim 24) is patentable under 35 U.S.C.§ 112, first paragraph.

The claim of group 10 provides a turbo decoding having a bit error rate not greater than 3 errors per 100,000 bits. In contrast, the Examiner rejected claim 24 asserting that the phrase "a bit error rate not greater than 2 errors per 10,000 bits" is not in the original specification.[3] Since the Examiner has rejected claim 24 based on language not found in claim 24, the rejection is inappropriate. As such, the claim of group 10 is fully compliant with the 35 U.S.C. §112, first paragraph, written description criteria and the rejection should be reversed.

B. 35 U.S.C. § 103

"[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[4] "[T]he factual inquiry whether to combine

---

[3] Office Action, October 22, 2003, page 2, section 2, lines 6-8.

[4] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

references must be thorough and searching."[5] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[6] "It must be based on objective evidence of record."[7] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations.[8] Furthermore, The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular".[9]

1. Group 1 (claims 1, 3, 4, 6, 8 and 9) is patentable over Citta and Yi.

The claims of group 1 provide a formatter configured to format a plurality of data frames of a transport stream by inserting a plurality of synchronization data to produce a block stream. The Examiner has asserted that a Data Source 24 of Citta is similar to the claimed formatter.[10] Assuming, *arguendo*, that the signal generated by the Data Source 24 of Citta is similar to the claimed block stream (for which Appellants' representative does not necessarily agree), Citta

---

[5] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[6] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[7] *Id.* at 1343, 61 USPQ2d at 1434.

[8] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revised February 2003, §2142.

[9] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)

[10] Office Action, October 22, 2003, page 3, section 4, part a.

appears to be silent regarding the Data Source 24 operating on a transport stream. Citta also appears to be silent regarding the Data Source 24 inserting a plurality of synchronization data into the data frames of the missing transport stream. Yi does not appear to cure the deficiencies of Citta. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a formatter configured to format a plurality of data frames of a transport stream by inserting a plurality of synchronization data to produce a block stream as presently claimed.

The claims of group 1 further provide an inserter configured to insert a synchronization signal into a data stream generated by an interleave module. In contrast, the Examiner has asserted that a Mapper and Sync Inserter 34 from FIG. 2A of Citta provides both (i) inserting synchronization data into the data frames of the missing transport stream operated on by the Data Source 24[11] and (ii) inserting a synchronization signal into a data stream generated by a combination of a Byte Interleaver 28 and Symbol Interleaver 30 of Citta.[12] However, the Examiner did not provide any explanation how the one Mapper and Sync Inserter 24 of Citta could operate on two different signals at the same time. Furthermore, one of ordinary skill in the art would appear to understand the Mapper and Sync Inserter 34 of Citta to operate only on a signal generated by an encoder as taught by Citta. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest both (i) a formatter configured to format a plurality of data frames of a transport stream by inserting a plurality of synchronization data to produce a block stream and (ii) an inserter configured to insert a synchronization signal into a data stream generated by an interleave module as presently claimed.

---

[11] Office Action, October 22, 2003, page 10, part b.

[12] Office Action, October 22, 2003, page 3, section 4, part e.

The claims of group 1 further provide a turbo encoder configured to encode the data stream. Assuming, *arguendo*, that it would have been obvious to modify Citta by replacing the Trellis Encoder 32 of Citta with the Turbo Encoder 502 of Yi as asserted by the Examiner[13] (for which Appellants' representative does not necessarily agree), the proposed combination does not appear to teach or suggest a turbo encoder operating on a stream having a synchronization signal. In particular, the Turbo Encoder 502 of Yi (in the Trellis Encoder 32 position of Citta) would appear to operate on data prior to a synchronization signal being added by the Mapper and Sync Inserter 34. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest both (i) an inserter configured to insert a synchronization signal into a data stream and (ii) a turbo encoder configured to encode the data stream as presently claimed.

The Examiner has not provided clear and particular evidence of motivation to combine the references. The Examiner has asserted that motivation to combine is:

> to minimize channel noise and fading, and make the operation of the system more efficient and reliable.[14]

However, no evidence has been provided that the asserted motivation comes from Citta, Yi or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Therefore, *prima facie* obviousness has not been established.

Furthermore, Appellants have provided evidence that a purpose of conventional convolution codecs is to convey signals through imperfect channels subject to noise and fading.[15]

---

[13] Office Action, page 4, lines 1-5.

[14] Office Action, October 22, 2003, page 4, lines 11-12.

[15] Amendment After Final, December 17, 2003, Appendix A, paragraph 9.4.1.

The Examiner has admitted that the Trellis Encoder 32 of Citta is a convolution encoder.[16] Therefore, one of ordinary skill in the art would not appear to view channel noise and fading as motivated to replace the Trellis Encoder 32 of Citta with the Turbo Encoder 502 of Yi since the Trellis Encoder 32 of Citta already appears to account for channel noise and fading. As such, the first half of the asserted motivation appears to be merely a conclusory statement.

A second half of the asserted motivation is to make the operation of the proposed combination "more efficient and reliable". However, no evidence has been provided that the Turbo Encoder 502 of Yi would improve efficiency and reliability relative to the Trellis Encoder 32 of Citta. Therefore, the asserted "more efficient and reliable" motivation also appears to be merely a conclusory statement. As such, *prima facie* obviousness has not been established to combine the references.

The Examiner has not provided evidence of a reasonable expectation of success for the proposed modification. In particular, the Examiner has not made any statements regarding the probability of the Turbo Encoder 502 of Yi operating in the system of Citta. Therefore, *prima facie obviousness* has not been established in accordance with M.P.E.P. §2142.

In summary, the Examiner has not established that the proposed combination of Citta and Yi teach or suggest (i) a formatter, (ii) an inserter and (ii) a turbo encoder as presently claimed. Furthermore, *prima facie* obviousness has not been established for lack of evidence of (i) motivation to combine the references and (ii) a reasonable expectation of success. As such, the claims of group 1 are fully patentable over the cited references and the rejection should be reversed.

---

[16] Office Action, October 22, 2003, page 4, lines 3-4.

2. Group 2 (claims 11 and 16) is patentable over Citta and Yi.

The claims of group 2 provide (i) a converter configured to convert a symbol stream comprising a plurality of symbols into an encoded stream and (ii) a turbo decoder configured to decode the encoded stream to produce a data stream. In contrast, the Examiner has asserted that a Postcoder 48 from FIG. 2A of Citta is similar to the claimed converter.[17] The Examiner has also asserts that it would have been obvious to replace a Viterbi Decoder 46 from FIG. 2A of Citta with a turbo decoder.[18] However, the Examiner has failed to provide any evidence that the Postcoder 48 of Citta has a reasonable expectation of operating successfully if positioned upstream of a turbo decoder. In particular, Citta states that the Postcoder 48 recovers estimations of input bits X1 and X2 from the Viterbi decoder 46.[19] Nothing in Citta appears to indicate that the Postcoder 48 can convert a symbol stream into an encoded stream that is decoded by a turbo decoder. The Examiner appears to be moving blocks around in FIG. 2A of Citta without regard for the corresponding functionality of the blocks or motivation to make the changes. Therefore, *prima facie* obviousness has not been established for lack of evidence for a reasonable expectation of success.

The claims of group 2 provide a turbo decoder configured to decoder an encoded stream to produce a data stream. In contrast, the Examiner has admitted that Citta does not teach or suggest a turbo decoder.[20] Furthermore, the Examiner has failed to provide clear and particular evidence of motivation to modify Citta to add a turbo decoder. The fact that references can be

---

[17] Office Action, October 22, 2003, page 5, lines 19-21.

[18] Office Action, October 22, 2003, page 6, lines 12-17.

[19] Citta, column 7, lines 10-13.

[20] Office Action, October 22, 2003, page 6, lines 3-4.

combined or modified is not sufficient to establish *prima facie* obviousness.[21] The Examiner has asserted motivation exists:

> in order to obtain better time delay, minimize noise, and signal fading, thereby make the over all operation of the system more efficient.[22]

However, the above asserted motivation does not appear to be based on Citta, Yi or knowledge generally available to one of ordinary skill in the art per M.P.E.P. §2142. Instead, the Examiner appears to have made a conclusory statement for motivation. Therefore, *prima facie* obviousness has not been established.

The claims of group 2 further provide a synchronization remover configured to remove a synchronization signal from a data stream. In contrast, Examiner has admitted that Citta does not teach or suggest a synchronization remover.[23] However, the Examiner has failed to provide clear and particular evidence of motivation to add a synchronization remover to Citta. Instead, the Examiner merely concludes that adding a synchronization remover would make the system "more efficient".[24] The asserted motivation does not appear to be based on Citta, Yi or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Furthermore, no explanation has been provided why the Symbol Deinterleaver 52, Byte Deinterleaver 54 or the Reed Solomon Decoder 56 of Citta would somehow operate more efficiently if a new circuit were added. As such, *prima facie* obviousness has not been established to modify Citta to include a synchronization remover as presently claimed.

---

[21] M.P.E.P., Eighth Edition, Revised February 2003, §1243.01.

[22] Office Action, October 22, 2003, page 6, lines 17-19.

[23] Office Action, October 22, 2003, page 6, lines 1-2.

[24] Office Action, October 22, 2003, page 6, lines 9-10.

The Examiner appears to have used the claims as templates for outlining the rejection. In particular, the combined teachings of Citta and Yi were only applied to one claimed element of group 2. The remaining claim elements where simply added and asserted to be "obvious" combinations. However, no evidence has been provided that (i) one of ordinary skill in the art would be motivated to add new elements with the claim limitations to the Post Coder 48 of Citta and (ii) there is a reasonable expectation for success to combine the Post Coder 48 with a turbo decoder and a synchronization remover. Therefore, *prima facie* obviousness has not been established.

In summary, the Examiner has admitted that Citta and Yi do not teach or suggest a turbo decoder and a synchronization remover as presently claimed. Furthermore, the Examiner has failed to establish (i) clear and particular evidence of motivation to modify Citta and Yi to include the missing turbo decoder and synchronisation remover and (ii) evidence of a reasonable expectation of success for the proposed modification. As such, *prima facie* obviousness has not been established and the rejection should be reversed.

3. Group 3 (claims 2 and 7) is patentable over Citta and Yi.

The claims of group 3 contains all of the limitations of group 1. Therefore, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 3.

The claims of group 3 further provide a transport stream that defines two high definition television programs substantially simultaneously. In contrast, Citta and Yi both appear to be silent regarding two high definition television programs in a signal substantially simultaneously. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest

a transport stream that defines two high definition television programs substantially simultaneously as presently claimed.

Furthermore, the Examiner has not provided any evidence in support of the assertion that a transport stream implies two high definition television programs substantially simultaneously.[25] In contrast, Appellants have provided evidence that digital broadcasting standards enable a single high definition television signal within a channel.[26] The Examiner has not traversed the evidence provided by the Appellants. Therefore, the Examiner has failed to establish that two high definition television programs taught or suggested by Citta and/or Yi. As such, the claims of group 3 are fully patentable over the cited references and the rejection should be reversed.

4. Group 4 (claim 21) is patentable over Citta and Yi.

The claim of group 4 contains all of the limitations of group 1. Therefore, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 4.

The claim of group 4 further provides a bit-to-symbol mapper configured to map an encoded stream to produce a symbol stream carrying a plurality of symbols each consisting of two error protected bits and one redundant bit. The Examiner has asserted that the Mapper and Sync Inserter 34 of Citta is similar to the claimed bit-to-symbol mapper. However, no evidence has been provided, and Citta appears to be silent regarding the Mapper and Sync Inserter 34 producing a plurality of symbols each **consisting** of two error protected bits and one redundant bit. Therefore,

---

[25] Office Action, October 22, 2003, page 4, lines 14-17.

[26] Amendment After Final, January 20, 2004, Appendix B.

Citta and Yi, alone or in combination, do not appear to teach or suggest a bit-to-symbol mapper configured to map an encoded stream to produce a symbol stream carrying a plurality of symbols each consisting of two error protected bits and one redundant bit as presently claimed.

Furthermore, the Examiner has asserted that the Mapper and Sync Inserter 34 of Citta is similar to all three of the claimed bit-to-symbol mapper as noted above, the claimed formatter[27] and the claimed inserter.[28] However, no evidence or explanation has been provided how the single Mapper and Sync Inserter 34 of Citta can operate on three different signals simultaneously. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest all of a formatter, an inserter and a bit-to-symbol mapper as presently claimed. As such, the claim of group 4 is fully patentable over the cited references and the rejection should be reversed.

5. Group 5 (claim 22) is patentable over Citta and Yi.

The claim of group 5 contains all of the limitations of group 1. Therefore, the arguments presented above in support of the patentability of group 1 are incorporated hereunder in support of group 5.

The claim of group 5 further provides a turbo encoder having a bit error rate not greater than 2 errors per 10,000 bits. In contrast, the Examiner has not provided any evidence, and both Citta and Yi appear to be silent regarding a bit error rate of an encoder. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a turbo encoder having a bit error rate

---

[27] Office Action, October 22, 2003, page 10, part b.

[28] Office Action, October 22, 2003, page 3, section 4, line e.

not greater than 2 errors per 10,000 bits as presently claimed. As such, the claim of group 5 is fully patentable over the cited references and the rejection should be reversed.

6. Group 6 (claims 12 and 17) is patentable over Citta and Yi.

The claim of group 6 contains all of the limitations of group 2. Therefore, the arguments presented above in support of the patentability of group 2 are incorporated hereunder in support of group 6.

The claims of group 6 further provide a transport stream that defines two high definition television programs substantially simultaneously. In contrast, Citta and Yi both appear to be silent regarding two high definition television programs in a signal substantially simultaneously. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a transport stream that defines two high definition television programs substantially simultaneously as presently claimed.

Furthermore, the Examiner has not provided any evidence in support of the assertion that a transport stream implies two high definition television programs substantially simultaneously.[29] In contrast, Appellants have provided evidence that digital broadcasting standards enable a single high definition television signal within a channel.[30] The Examiner has not traversed the evidence provided by the Appellants. Therefore, the Examiner has failed to establish that two high definition television programs taught or suggested by Citta and/or Yi. As such, the claims of group 6 are fully patentable over the cited references and the rejection should be reversed.

---

[29] Office Action, October 22, 2003, page 4, lines 14-17.

[30] Amendment After Final, January 20, 2004, Appendix B.

7. Group 7 (claims 13 and 18) is patentable over Citta and Yi.

The claims of group 7 contain all of the limitations of group 2. Therefore, the arguments presented above in support of the patentability of group 2 are incorporated hereunder in support of group 7.

The claims of group 7 further provide a plurality of decode modules configured to decode a stream to produce a data stream. In contrast, the Examiner has not provided any evidence, and both Citta and Yi appear to be silent regarding internal operations of a turbo decoder. Therefore, Citta, and Yi, alone or in combination, do not appear to teach or suggest a plurality of decode modules configured to decode a stream to produce a data stream as presently claimed. As such, claims of group 7 are fully patentable over the cited references and the rejection should be reversed.

8. Group 8 (claims 14 and 19) is patentable over Citta and Yi.

The claims of group 8 contains all of the limitations of group 2. Therefore, the arguments presented above in support of the patentability of group 2 are incorporated hereunder in support of group 8.

The claims of group 8 further provide a de-puncture module configured to de-puncture a redundant portion of an encoded stream. In contrast, the Examiner has not provided any evidence, and both Citta and Yi appear to be silent regarding de-puncture modules. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a de-puncture module configured to de-puncture a redundant portion of an encoded stream as presently claimed. As such, the claims of group 8 are fully patentable over the cited references and the rejection should be reversed.

9. Group 9 (claim 23) is patentable over Citta and Yi.

The claim of group 9 contains all of the limitations of group 2. Therefore, the arguments presented above in support of the patentability of group 2 are incorporated hereunder in support of group 9.

The claim of group 9 further provides a demodulator configured to demodulate a signal to produce a symbol stream wherein each of the symbols consists of two error protected bits and one redundant bit. Despite the assertion by the Examiner[31], FIG. 2A of Citta appears to be silent regarding a Tuner Demod A/D circuit 40 generating a demodulated stream of symbols where each symbol consists of two error protection bits and one redundant bit. Yi does not appear to cure the deficiency of Citta. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a demodulator configured to demodulate a signal to produce a symbol stream wherein each of the symbols consists of two error protected bits and one redundant bit as presently claimed. As such, the claim of group 9 is fully patentable over the cited reference and the rejection should be reversed.

10. Group10 (claim 24) is patentable over Citta and Yi.

The claim of group 10 contains all of the limitations of group 2. Therefore, the arguments presented above in support of the patentability of group 2 are incorporated hereunder in support of group 10.

The claim of group 10 further provides a bit error rate not greater than 3 errors per 100,000 bits for decoding. In contrast, the Examiner has not provided any evidence, and both Citta

---

[31] Office Action, October 22, 2003, page 8, lines 7-8.

and Yi appear to be silent regarding bit error rates. Therefore, Citta and Yi, alone or in combination, do not appear to teach or suggest a bit error rate not greater than 3 errors per 100,000 bits for decoding as presently claimed. As such, claim of group 10 is fully patentable over the cited reference and the rejection should be withdrawn.

Groups 1-10 are separately patentable.

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[32] As such, each of the above groups is considered to be separately patentable over every other group.[33] In particular, each of the groups includes a unique combination of arguments that allow individual groups to stand over the references even if all of the other groups fall.

Group 2 includes an argument that Citta and Yi do not teach or suggest a turbo decoder as presently claimed. Since group 1 does not depend on the turbo decoder argument, group 2 may be found patentable even if group 1 is not.

Group 3 includes an argument that Citta and Yi do not teach or suggest an encoder operating on two high definition programs substantially simultaneously as presently claimed. Since groups 1-2 do not depend on the encoding of two high definition programs argument, group 3 may be found patentable even if groups 1 and/or 2 are not.

---

[32] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[33] M.P.E.P., Eighth Edition, Revised February 2003, §1206.

Group 4 includes an argument that Citta and Yi do not teach or suggest a bit-to-symbol mapper as presently claimed. Since groups 1-3 do not depend on the bit-to-symbol mapper argument, group 4 may be found patentable even if groups 1-2 and/or 3 are not.

Group 5 includes an argument that Citta and Yi do not teach or suggest 2 error per 10,000 bits as presently claimed. Since groups 1-4 do not depend on the bit error rate argument, group 5 may be found patentable even if groups 1-3 and/or 4 are not.

Group 6 includes an argument that Citta and Yi do not teach or suggest a decoder operating on two high definition programs substantially simultaneously as presently claimed. Since groups 1-5 do not depend on the decoding of two high definition programs argument, group 6 may be found patentable even if groups 1-4 and/or 5 are not.

Group 7 includes an argument that Citta and Yi do not teach or suggest a plurality of decoder modules as presently claimed. Since groups 1-6 do not depend on the decoder module argument, group 7 may be found patentable even if groups 1-5 and/or 6 are not.

Group 8 includes an argument that Citta and Yi do not teach or suggest a de-puncture module as presently claimed. Since groups 1-7 do not depend on the de-puncture module argument, group 8 may be found patentable even if groups 1-6 and/or 7 are not.

Group 9 includes an argument that Citta and Yi do not teach or suggest symbols consisting of two error protected bits and one redundant bit as presently claimed. Since groups 1-8 do not depend on the symbol argument, group 9 may be found patentable even if groups 1-7 and/or 8 are not.

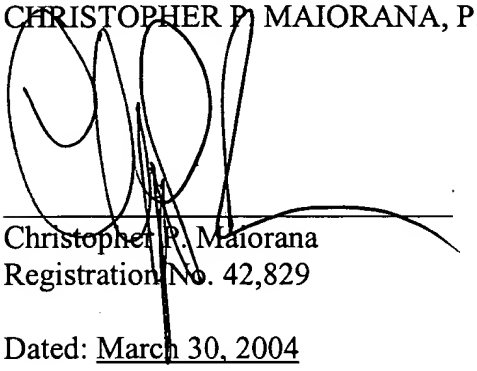
Group 10 includes an argument that Citta and Yi do not teach or suggest 3 errors per 100,000 bits as presently claimed. Since groups 1-9 do not depend on the bit error rate argument, group 10 may be found patentable even if groups 1-8 and/or 9 are not.

C. CONCLUSION

The Examiner has failed to establish that Citta and Yi, alone or in combination, teach or suggest (i) a encoder system comprising a formatter, an inserter and a turbo encoder and (ii) a decoder system comprising a converter, a turbo decoder and a synchronization remover as presently claimed. Furthermore, the Examiner has not established *prima facie* obviousness for lack of (i) clear and particular evidence of motivation to combine the references and (ii) evidence of a reasonable expectation of success for the various proposed combinations. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited references. However, should the Board find the arguments herein in support of independent claims 1, 6, 11 and/or 16 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Christopher P. Maiorana
Registration No. 42,829

Dated: March 30, 2004

c/o Leo Peters
Intellectual Property Law Department
LSI Logic Corporation
1621 Barber Lane
MS: D-106 Legal
Milpitas, CA 95035

IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. A system comprising:

a formatter (102) configured to format a plurality of data frames of a transport stream by inserting a plurality of synchronization data to produce a block stream;

an error correction encoder (104) configured to encode said block stream to produce an error protected block stream;

an interleave module (106) configured to interleave said error protected block stream to produce a data stream;

an inserter (108) configured to insert a synchronization signal into said data stream; and

a turbo encoder (110) configured to encode said data stream to produce an encoded stream.

2. The system according to claim 1, wherein said transport stream defines two high definition television programs substantially simultaneously.

3. The system according to claim 1, wherein said turbo encoder comprises:

a first systematic encoder (802) configured to encode said data stream to produce a first redundant stream;

a bit interleave module (806) configured to interleave said data stream to produce a second data stream; and

a second systematic encoder (804) configured to encode said second data stream to produce a second redundant stream.

4. The system according to claim 3, wherein said turbo encoder further comprises:

a puncture module configured to puncture bits from said first redundant stream and said second redundant stream to produce a redundant portion of said encoded stream.

5. (CANCELED)

6. A method for transmitting comprising the steps of:

(A) formatting a plurality of data frames of a transport stream by inserting a plurality of synchronization data to produce a block stream;

(B) error correction encoding said block stream to produce an error protected block stream;

(C) interleaving said error protected block stream to produce a data stream;

(D) inserting a synchronization signal into said data stream; and

(E) turbo encoding said data stream to produce an encoded stream.

7. The method according to claim 6, wherein said transport stream defines two high definition television programs substantially simultaneously.

8. The method according to claim 6, further comprising the steps of:

encoding said data stream to produce a first redundant stream;

interleaving said data stream to produce a second data stream; and

encoding said second data stream to produce a second redundant stream.

9. The method according to claim 8, further comprising the step of:

puncturing bits from said first redundant stream and said second redundant stream to produce a redundant portion of said encoded stream.

10. (CANCELED)

11. A system comprising:

a converter (1204) configured to convert a symbol stream comprising a plurality of symbols into an encoded stream;

a turbo decoder (1206) configured to decode said encoded stream to produce a data stream; and

a synchronization remover (1208) configured to remove a synchronization signal from said data stream.

12. The system according to claim 11, wherein said symbol stream defines two high definition television programs substantially simultaneously.

13. The system of claim 11, wherein said turbo decoder comprises:

a plurality of decode modules configured to decode said encoded stream to produce said data stream.

14. The system according to claim 13, wherein said turbo decoder further comprises:

a de-puncture module configured to de-puncture a redundant portion of said encoded stream.

15. (CANCELED)

16. A method for receiving comprising the steps of:

(A) converting a symbol stream comprising a plurality of symbols into an encoded stream;

(B) turbo decoding said encoded stream to produce a data stream; and

(C) removing a synchronization signal from said data stream.

17. The method according to claim 16, wherein said symbol stream defines two high definition television programs substantially simultaneously.

18. The method according to claim 16, wherein step (B) further comprises the sub-step of:

decoding said encoded stream in a plurality of modules to produce said data stream.

19. The method according to claim 18, further comprising the step of;

de-puncturing a redundant portion of said encoded stream.

20. (CANCELED)

21. The system according to claim 1, further comprising:

a bit-to-symbol mapper configured to map said encoded stream to produce a symbol stream carrying a plurality of symbols each consisting of two error protected bits and one redundant bit.

22. The method according to claim 6, wherein said turbo encoding has a bit error rate not greater than 2 errors per 10,000 bits.

23. The system according to claim 11, further comprising:

a demodulator configured to demodulate a signal to produce said symbol stream wherein each of said symbols consists of two error protected bits and one redundant bit.

24. The method according to claim 16, wherein said turbo decoding has a bit error rate not greater than 3 errors per 100,000 bits.